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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,576	07/18/2003	Cheol-Joon Yoo	2557-000157/US	2118

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EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,576	YOO ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 01 November 2004.

Specification

1. The disclosure is objected to because of the following informalities:

In paragraph [0003], line 9, change "from" to --form-- to correct spelling; and

In paragraph [0031], line 4, change "203" to --204-- because the wafer is designated as reference number 204 (see Fig. 7 and paragraph [0030], first sentence).

Appropriate correction is required. It is noted that the amendment filed on 01 November 2004 refers to an amendment to the specification that begins on page 2. However this amendment to the specification is not present in the file of record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Garrett, Sr. et al. (US 4,285,433).

Referring to Figs. 1, 2 and column 3, line 64 to column 4, line 48, Garrett, Sr. et al. disclose an apparatus for removing semiconductor dice (16) from a bi-layer of tape (12, 14). The apparatus includes an adhesive tape (18) that is pulled across a surface (20) to convey a diced wafer (10) that is positioned thereon. The dice (16) are affixed to two layers of tape (12, 14) with one layer (12) adhered to the dice (16) and the other layer (14) adhered to the adhesive tape (18). The tape layers (12, 14, 18) are pulled over an edge (24) and through a slot (38), which causes the dice (16) to separate from the one layer of tape (12) because the other layer (14) and the adhesive layer (18) have greater adhesive strengths than the one layer (12). These are all of the limitations set forth in claim 14 of the applicant's invention.

Regarding claim 15, the adhesive tape (18) is pulled from a supply roll (22) across the surface (20), over the edge (24) and onto a take-up reel (26).

Regarding claim 16, the adhesive tape (18) is pulled with a crank (32) that is used to turn the take-up reel (26). The take-up reel (26) performs the functions of both a guide roller and a pressure roller.

Regarding claim 17, the entire diced wafer (10) is mounted on the adhesive tape (18).

4. Claims 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth et al. (US 6,202,292 B1).

Referring to Figs. 1a, 1b and column 5, line 7 to column 6, line 7, Farnworth et al. disclose a frame (106) for supporting a carrier tape (104) that has a diced wafer (101) comprising singulated die (102a, 102b, etc.) mounted thereon. The frame (106) is connected to a base (110) of an apparatus (100). The apparatus (100) also includes a screen (112) positioned over a plate member (120) and a vacuum source (114) connected to the base (110) beneath the plate member (120). The vacuum source (114) is activated to provide suction through the screen (112), which causes the carrier tape (104) to pull away from the singulated die (102a, 102b, etc.). These are all of the limitations set forth in claims 19-21 of the applicant's invention.

5. Claims 1-3, 5-6, 8-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawakami (US 2003/0190795 A1).

Referring to Figs. 3-11, Kawakami discloses an embodiment of a packaging method for mounting semiconductor chips on a wiring substrate with the following features:

- A transparent protective tape (15) with a thickness of about 100 μm is affixed to the main surface of a semiconductor wafer (3a) as shown in Fig. 3 (also see paragraph [0051]);
- The main surface of the wafer (3a) is patterned into rectangular chip portions and includes dicing (i.e. scribe) lines (also see paragraph [0049]);
- Then the backside of the wafer (3a) undergoes a grinding process to reduce the wafer thickness to 100 μm as indicated by the dotted line in Fig. 3 (also see paragraph [0054]);
- Then the back side of the wafer (3a) is affixed to dicing tape (16) which is supported by an outer frame (17) as shown in Fig. 4 and a dicing blade (18) is used to saw the wafer (3a) into individual chips (3) as shown in Fig. 5 (also see paragraphs [0055] to [0058]);
- Then the chips (3) are transported to the wiring substrate (2a) and bonded to chip fixing portions (i.e. chip pads) of the wiring substrate (2a) while portions of the protective tape (15) remain on the main surface of the chips as shown in Fig. 7 (also see paragraphs [0059] to [0063]);
- Then the protective tape (15) is removed by a variety of peeling means that can include using uv radiation to weaken the bonding force of the tape prior to the peeling step (also see paragraphs [0066] and [0074]); and
- Bump electrodes (6) are formed on the bottom surface of the wiring substrate (2 in Fig. 1) (also see paragraphs [0045] and [0078]).

These are all of the limitations set forth in claims 1-3, 5-6, 8-11 of the applicant's invention.

Regarding claim 12 and the apparatus claims 19-22, one of the peeling means for removing the protective tape (15), as shown in Fig. 9(b), uses a vacuum suction jig (36) by placing nozzles (35) in contact with the protective tape (15), applying vacuum (37) to hold the tape (15), and moving the jig (36) away from wiring substrate (2a) (also see paragraph [0071] to [0072]).

Regarding claim 13 and the apparatus claims 14-18, another of the peeling means for removing the protective tape (15), as shown in Fig. 9(a), applies an adhesive tape (32) to the protective tape (15) corresponding to a chip (3), bonding the adhesive tape (32) to the protective tape (15), and separating the adhesive tape (32) from the chip (3) resulting in peeling the protective tape (15) from the chip (3) (also see paragraphs [0067] to [0070]). The apparatus includes a tape unwind reel (30), a tape take-up reel (31), and a movable roller (33) to push the adhesive tape (32) against the protective tape.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6, 8-11, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 6,297,131 B1) in view of Huang et al. (US 6,650,006 B2).

Referring to Figs. 8-13 and column 5, line 20 to column 8, line 6, Yamada et al. disclose a method for thinning and dicing a wafer that includes the following features:

- A protective tape (32) is applied to the front surface (i.e. the active circuit side) of a semiconductor wafer (30) and the opposite side of the protective tape is then mounted on a layer of dicing tape (36) that is supported by a frame (34) as shown in Fig. 8;
- The protective tape is a 150 μm thick layer of polyethylene with about 30 to 40 μm of UV curable pressure sensitive adhesive in direct contact with the wafer (30);
- The back side of the wafer is then thinned with grinding tool (38) to a thickness of less than 200 μm and as thin as 50 μm as shown in Fig. 9;

- The wafer (30) is then diced along scribe lines into a plurality of semiconductor chips (30A) using a dicing saw (42) as shown in Fig. 11;
- The UV curable pressure sensitive adhesive is then cured by transmitting UV light through the dicing tape (36) and the protective tape (32) to the front surface of the chips (30A) as shown in Fig. 12 resulting in a reduction of adhesive force between the protective tape (32) and the chips (30A);
- The fact that UV light transmits through both the dicing tape (36) and the protective tape (32) implies that both tapes are transparent to visible light; and
- The chips (30A) are individually separated from the protective tape (32) by pushing a pin (46A) against the back surface of the dicing tape (36) to bend the protective tape (32) directly under one chip (30A) while using a vacuum pickup (44) to pull the one chip (30A) away from the protective tape (32) as shown in Fig.13.

These are limitations set forth in claims 1-3, 6, 8-11, 13 of the applicant's invention.

However, Yamada et al. lack the step of attaching an individual chip to a chip pad, which is a limitation of applicant's claim 1. More specifically, Yamada et al. do not teach or suggest providing the chip pad on a lead frame with outer leads for making external connections (the limitations of claim 4), nor do they teach or suggest providing the chip pad on a substrate with solder balls for making external connections (the limitations of claim 5).

Huang et al. teach that chips can be mounted on a chip carrier, which can be a die pad of a conventional lead frame comprising corresponding leads for electrically

connecting the chip to external devices or, which can be a substrate with solder balls for electrically connecting the chip to external devices (see column 3, line 54 to column 4, line 11).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada et al. and Huang et al. in order to attach the separated chip of Yamada et al. to a chip carrier as taught by Huang et al. Huang et al. recognize that lead frames and substrates with solder ball connections are known in the art as conventional ways of electrically connecting semiconductor chips to external devices (see column 3, line 66 to column 4, line 8).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 6,297,131 B1) and Huang et al. (US 6,650,006 B2) as applied to claim 1 above, and further in view of Oka (US 2002/0048904 A1).

As shown above, the combination of Yamada et al. and Huang et al. has all of the limitations set forth in claim 1 of the applicant's invention. However, this combination lacks the further limitation to claim 1 set forth in claim 7 of the applicant's invention, which is to heat the protective tape above a degradation temperature. Oka teaches that a protective tape using thermoplastic resin as an adhesive can be peeled off from a wafer after heating the resin to lower its adhesiveness (see paragraph [0039]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined teachings of Yamada et al. and

Huang et al. by using a protective tape with a thermoplastic resin adhesive, as taught by Oka, in order to release the protective tape from the chips of Yamada et al. by heating. Oka recognizes that applying heat to thermoplastic resin adhesive to lower the adhesiveness of protective tape has the equivalent effect of applying UV light to a UV curable adhesive (see paragraph [0039]).

Response to Arguments

9. Applicant's arguments filed 01 November 2004 (see pages 9-13) have been fully considered but they are not persuasive.

In response to applicant's argument regarding the above rejection of claims 14-17 under 35 U.S.C. 102(b) that Garrett, Sr. et al. (US 4,285,433) lack the limitation of removing a protective tape portion from a protected surface of an individual chip while the individual chip is attached to a chip pad, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Accordingly, the apparatus disclosed by Garrett, Sr. et al. is capable of performing the function of separating protective tape from an individual chip while the individual chip is attached to a chip pad (also see MPEP section 2114).

In response to applicant's argument regarding the above rejection of claims 19-21 under 35 U.S.C. 102(b) that Farnworth et al. (US 6,202,292 B1) lack the limitation of removing a protective tape portion from a protected surface of an individual chip while the individual chip is attached to a chip pad, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Accordingly, the apparatus disclosed by Farnworth et al. is capable of performing the function of separating protective tape from an individual chip while the individual chip is attached to a chip pad (also see MPEP section 2114).

Regarding the above rejection of claims 1-3, 5-6, 8-22 under 35 U.S.C. 102(e) as being anticipated by Kawakami (US 2003/0190795 A1), the applicant's intention to provide an English translation of the Korean priority document (KR 2002-82672 filed on 23 December 2002) is acknowledged. However, like the amendment to the specification, this translation is not present in the file of record.

Regarding the above rejection of claims 1-11, 13 under 35 U.S.C. 103(a) as being unpatentable either partially (claim 7) or wholly (claims 1-6, 8-11, 13) over the combined teachings of Yamada et al. (US 6,297,131 B1) and Huang et al. (US 6,650,006 B2), the applicant contends that there is no suggestion to combine the references. The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Huang et al. provide motivation for the combination because they recognize that lead frames and substrates with solder ball connections are known in the art as conventional ways of electrically connecting semiconductor chips to external devices (see column 3, line 66 to column 4, line 8).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813